IN THE CLAIMS

Please cancel claims 4, 12 and 16 – 20.

Please amend the claims to read as indicated herein.

1. (currently amended) An automated test equipment (ATE) comprising:

a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT) having a plurality of DUT pins, and wherein, during a testing sequence, said DUT is defined as (a) a first DUT core that represents a first functional unit of said DUT and (b) a second DUT core that represents a second functional unit of said DUT;

an assigning component that assigns, during said testing sequence, (a) a first subset of said plurality of per-pin testing units to ~~an~~ a first ATE-port, for interfacing with said first DUT core via a first subset of said plurality of DUT pins, and (b) a second subset of said plurality of per-pin testing units to a second ATE-port, for interfacing with said second DUT core via a second subset of said plurality of DUT pins; and

a programming component that (a) obtains a first specification for testing said first DUT core, prepares a first program based on said first specification, and programs said first ATE-port with said first program, and (b) obtains a second specification for testing said second DUT core, prepares a second program based on said second specification, and programs said second ATE-port with said second program,

wherein said ~~program defines at least one of programming timing or a stimulus/response pattern, and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port, and wherein each waveform represents a sequence of events of various types occurring at specified instances in time~~ first and

second ATE-ports are sequenced independently of one another during execution of said first and second programs.

2. (currently amended) The automated test equipment of claim 1, wherein said assigning component comprises:

a component that switches connections between one or more of said plurality of per-pin testing units and one or more of said plurality of DUT pins; and

a component that controls said switching in accordance with said assigning of said ~~subset~~ first and second subsets of said plurality of per-pin testing units.

3 - 4. (canceled)

5. (previously presented) The automated test equipment of claim 1, wherein said programming component comprises:

main pattern programs for implementing access protocols to said first DUT core.

6. (currently amended) The automated test equipment of claim 5, wherein said main pattern program comprises at least one of:

a component that configures said first ATE-port for activating said first subset of said plurality of per-pin testing units for accessing said first DUT core; and

a component that selects pattern data generated by pattern programs of said first DUT core during one testing sequence for testing said first DUT core.

7. (currently amended) The automated test equipment of claim 1, wherein said programming component comprises:

a component that defines an alias mapping between said plurality of per-pin testing units for a plurality of ATE-ports, and specifies at least one of timing information and a pattern program of said first ATE-port to apply for said plurality of ATE-ports for which said alias mapping is defined.

8. (previously presented) The automated test equipment according to claim 1, further comprising a component that specifies overall test conditions for a test that concurrently operates on multiple ATE-ports.

9. (previously presented) The automated test equipment of claim 8, wherein said component that specifies overall test conditions comprises at least one of:

a component that determines a set of concurrently active ATE-ports during a defined testing sequence;

a component that selects ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins;

a component that specifies global test conditions to express dependencies between pins of said DUT and said ATE; and

a component that determines a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

10. (currently amended) A method for testing a device under test (DUT) with automated test equipment (ATE) having a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of said DUT, said method comprising:

defining, for a testing sequence, (a) a first DUT core that represents a first functional unit of said DUT, and (b) a second DUT core that represents a second functional unit of said DUT;

assigning, during said testing sequence, (a) a first subset of said plurality of per-pin testing units to ~~an~~ a first ATE-port, for interfacing with said first DUT core via a first subset of said plurality of DUT pins, and (b) a second subset of said plurality of per-pin testing units to a second ATE-port, for interfacing with said second DUT core via a second subset of said plurality of DUT pins;

obtaining a first specification for testing said first DUT core, and a second specification for testing said second DUT core;

preparing a first program based said first specification, and a second program based on said second specification; and

programming said ATE-port with said first program, and said second ATE-port with said second program,

wherein said ~~program defines at least one of programming timing or a stimulus/response pattern for said ATE-port, and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port, and wherein each waveform represents a sequence of events of various types occurring at specified instances in time~~ first and second ATE-ports are sequenced independently of one another during execution of said first and second programs.

11 - 12. (canceled)

13. (previously presented) The method according to claim10, further comprising:

specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

14. (previously presented) The method of claim 13, wherein specifying overall test conditions comprises:

determining a set of concurrently active ATE-ports during a defined testing sequence;

selecting ATE-port test conditions for one or more ATE-pins;

specifying global test conditions to express dependencies between pins of said DUT and said ATE; and

determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

15. (currently amended) A data media for storing computer instructions for automated test equipment, said data media comprising:

instructions for testing a device under test (DUT) with automated test equipment (ATE) having a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units has circuitry for at least one of emitting a

signal to, or receiving a signal from, a pin of said DUT, wherein said DUT includes a plurality of DUT pins;

instructions for defining, for a testing sequence, (a) a first DUT core that represents a first functional unit of said DUT, and (b) a second DUT core that represents a second functional unit of said DUT~~;; and~~; and

instructions for assigning, during said testing sequence, (a) a first subset of said plurality of per-pin testing units to ~~an~~ a first ATE-port, for interfacing with said first DUT core via a first subset of said plurality of DUT pins, and (b) a second subset of said plurality of per-pin testing units to a second ATE-port, for interfacing with said second DUT core via a second subset of said plurality of DUT pins;

instructions for obtaining a first specification for testing said first DUT core, and a second specification for testing said second DUT core;

instructions for preparing a first program based said first specification, and a second program based on said second specification; and

instructions for programming said first ATE-port with ~~a~~ said first program ~~for testing said first DUT core~~, and said second ATE-port with said second program,

wherein said ~~program defines at least one of programming timing or a stimulus/response pattern for said ATE port, and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE port, and wherein each waveform represents a sequence of events of various types occurring at specified instances in time~~ first and second ATE-ports are sequenced independently of one another during execution of said first and second programs.

16 – 20. (canceled)

Please add the following claims, newly numbered as claims 21 - 24.

21. (new) The automated test equipment of claim 1, wherein said first ATE-port sequences through branching conditions of said first program, independently of sequencing by said second ATE-port.

22. (new) The automated test equipment of claim 1, wherein each of said first subset of said plurality of per-pin testing units includes an interface for communicating with interfaces of other per-pin testing units of said first subset.

23. (new) An automated test equipment (ATE) system, comprising a first per-pin testing unit that includes:

circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT);

a processor for controlling said circuitry; and

an interface coupled to said processor, for communicating with an interface of a second per-pin testing unit,

wherein said communicating enables said processor to co-operate with a processor of said second per-pin testing unit for testing said DUT.

24. (new) The ATE system of claim 23,

wherein said first and second per-pin testing units are assigned to a first ATE-port to execute a first program for testing a first functional unit of said DUT,

wherein said ATE system further comprises a third per-pin testing unit assigned to a second ATE-port to execute a second program for testing a second functional unit of said DUT, and

wherein said first and second ATE-ports are sequenced in parallel with, but independently of, one another.